AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A method of manufacturing a semiconductor device, the method comprising:

forming a transistor having a gate structure over a substrate with a gate dielectric layer therebetween;

forming an interlayer dielectric over the transistor; and

forming a silicon-rich silicon oxide layer, having a refractive index (R.I.)greater than 1.6, on an upper surface of the interlayer dielectric.

2. (Withdrawn) The method according to claim 1, comprising forming the silicon-silicon rich oxide layer with a RI greater than 1.7.

3. (Withdrawn) The method according to claim 2, comprising forming the silicon-rich silicon oxide layer with a R.I. of 1.7 to 2.0.

4. (Withdrawn) The method according to claim 2, comprising forming the silicon-rich silicon oxide layer at a thickness of 400 Å to 600 Å.

5. (Withdrawn) The method according to claim 1, comprising:

depositing a layer of boron-phosphorous-doped silicate glass (BPSG) as the interlayer dielectric;

planarizing the upper surface of the BPSG layer; and

depositing the silicon-rich silicon oxide layer by chemical vapor deposition.

6. (Withdrawn) The method according to claim 1, comprising depositing the silicon-rich silicon oxide layer by plasma enhanced chemical vapor deposition at a temperature of 450°C to 650°C.

7. (Withdrawn) The method according to claim 6, comprising depositing the silicon-rich silicon oxide layer at a silane flow rate of 100 to 150 sccm.

8. (Withdrawn) The method according to claim 7, comprising depositing the silicon-rich silicon oxide layer at:

an N_2O flow rate of 165 to 195 sccm;

an R.F. power of 110 to 140 watts;

a spacing of 625 to 675 mils; and

a pressure of 1.8 to 2.2 Torr.

9. (Withdrawn) The method according to claim 8, comprising depositing the silicon-rich silicon oxide layer for 3 to 15 seconds.

10. (Withdrawn) The method according to claim 1, wherein the gate structure comprises:

a tunnel oxide as the gate dielectric layer on the substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate electrode on the interpoly dielectric.

11. (Withdrawn) The method according to claim 10, comprising:

forming silicon oxide sidewall spacers on the side surfaces of the gate structure;

forming a layer of silicon nitride on an upper surface of the gate stack and on the silicon oxide sidewall spacers; and

thereafter depositing the interlayer dielectric.

Please Enter 12-10 Currently Amended

12. (Currently Amended) A semiconductor device comprising:

a transistor having a gate structure over a substrate with a gate dielectric layer therebetween;

an interlayer dielectric over the transistor and substrate; and

a silicon-rich silicon oxide layer, ~~having~~ which is substantially opaque to UV radiation and has a refractive index (R.I.) greater than 1.6, on an upper surface of the interlayer dielectric.

13. (Original) The semiconductor device according to claim 12, wherein the silicon-rich silicon oxide layer has a R.I. greater than 1.7.

14. (Original) The semiconductor device according to claim 13, wherein the silicon-rich silicon oxide layer has a R.I. of 1.7 to 2.0.

15. (Previously Presented) The semiconductor device according to claim 12, wherein the silicon-rich silicon oxide layer has a thickness of 400Å to 600Å.

16. (Original) The semiconductor device according to claim 12, wherein the gate structure comprises:

a tunnel oxide as the gate dielectric layer on the substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate electrode on the interpoly dielectric.

17. (Original) The semiconductor device according to claim 16, comprising silicon oxide sidewall spacers on side surfaces of the gate structure.

18. (Original) The semiconductor device according to claim 17, comprising a layer of silicon nitride on an upper surface of the gate structure and on the silicon oxide sidewall spacers.

19. (Original) The semiconductor device according to claim 12, wherein the interlayer dielectric comprises a boron-phosphorous-doped silicate glass (BPSG).

20. (Cancelled)

telephonic interview of January 24, 2005, the Examiner agreed that the present Amendment would overcome the imposed rejections.

Applicants would stress that, for the reasons expressed in the responsive Amendment submitted November 16, 2004, one having ordinary skill in the art would not have been realistically motivated to modify the semiconductor device disclosed by Alluri et al. by providing a silicon-rich silicon oxide layer having an RI greater than 1.6 as specified in claim 12 prior to the present Amendment. At any rate, in order to expedite prosecution, claim 12 has been amended by incorporating the limitations of claim 20 therein, thereby requiring the silicon-rich silicon oxide layer to be substantially opaque to UV radiation. This concept is neither disclosed by Alluri et al. or Cheung. Accordingly, even if the applied references are combined as suggested by the Examiner, and Applicants do not agree that the requisite fact-based motivation ahs been established, the **claimed invention** would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).*

Applicants, therefore, submit that the imposed rejection of claims 12 through 15 under 35 U.S.C. § 103 for obviousness predicated upon Alluri et al. in view of Cheung is not factually or legally viable and, hence, solicit withdrawal thereof.

Claims 16 through 19 were rejected under 35 U.S.C. § 103 for obviousness predicated upon Alluri et al. in view of Cheung, Weimer and Wolf et al.

This rejection is traversed. Specifically, claims 16 through 19 depend from independent claim 12. Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 12 under 35 U.S.C. § 103 for obviousness predicated upon Alluri et al. in view of Cheung. The additional references to Weimer and Wolf et al. do not cure the